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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,213	07/02/2008	Wolfgang Fey	AP 10793	6892

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Craig Hallacher
Continental Teves, Inc.
One Continental Drive
Auburn Hills, MI 48326

EXAMINER	
ALGAHAIM, HELAL A	
ART UNIT	PAPER NUMBER
3663	

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12/19/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,213	FEY ET AL.	
	Examiner	Art Unit	
	HELAL A. ALGAHAIM	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *9-16* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *9-16* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **9-11 and 14-16** are rejected under 35 U.S.C. 102(**b**) as being anticipated by **Giers (WO 98/48326), note: the Examiner used US equivalent patent (US 6823251) for citations**.

Regarding claim 9, Giers discloses an integrated circuit arrangement for safety-critical applications, for controlling tasks in an electronic brake system for motor vehicles, comprising: a plurality of electronic, cooperating functional groups (25, 25'); and a plurality of electric lines (30) provided to interconnect the functional groups (25, 25'), wherein the functional groups includes groups of a first type and second type, with the functional groups of the first type comprising a functional group redundant microprocessor system (1) and the functional group input/output devices (19), and the functional groups of the second type comprising the functional groups actuator drivers (11, 15, 24, 35) and safety circuits (5, 5', 7, 7'), and with the functional groups of the first type and the second type being grouped on a joint chip or chip support member (at least abstract, fig. 1 and col. 4, lines 1-31).

Claims **9-11 and 14-16** are rejected under 35 U.S.C. 102(**b**) as being anticipated by **Adrian et al (WO 03050624).**

Regarding claim 9, Adrian et al disclose an integrated circuit arrangement for safety-critical applications, for controlling tasks in an electronic brake system for motor vehicles, comprising:

a plurality of electronic, cooperating functional groups (25, 25'); and a plurality of electric lines (30) provided to interconnect the functional groups (25, 25'), wherein the functional groups includes groups of a first type and second type, with the functional groups of the first type comprising a functional group redundant microprocessor system (1) and the functional group input/output devices (19), and the functional groups of the second type comprising the functional groups actuator drivers (11, 15, 24, 35) and safety circuits (5, 5', 7, 7'), and with the functional groups of the first type and the second type being grouped on a joint chip or chip support member (at least translated abstract).

Regarding claim 10, the integrated circuit arrangement according to claim 9, wherein the redundant microprocessor system is a core-redundant microcontroller system or a microcontroller system with a symmetrical redundancy or a microcontroller system with asymmetrical redundancy (at least see Adrian, abstract OR Giers, abstract and fig. 1).

Regarding claim 11, the integrated circuit arrangement according to claim 9, wherein the functional groups are protected against one another at least partly by isolated areas, wherein the isolated areas are doped guard rings or etched barriers such as trenches or deep trenches.

Regarding claim 14, the integrated circuit arrangement according to claim 9, wherein the microprocessor system cross-links the functional groups of the first type, which comprise

substantially digital circuit components, and the functional groups of the second type, which substantially comprise analog circuit components for actuating efficient consumers, and in particular the safety circuits in such a fashion that individual safety monitoring of the single functional groups is rendered possible (at least see Adrian, fig. 1 OR Giers, fig. 1).

Regarding claim 15, the integrated circuit arrangement according to claim 9, wherein part of the functional groups is redundantly designed two times or more times (5, 5'), and in the event of malfunction of the redundantly designed functional group (5), another equal functional group (5') assumes the function of the faulty functional group, and signal lines (37, 38) and logic components (34) are provided for this purpose which either cause disabling of the faulty function (fault silent) or ensure switch-over of the function to the faultlessly functioning functional group (5') (fault tolerant) (at least see Giers abstract col. 5, lines 34-51).

Regarding claim 16, the integrated circuit arrangement according to claim 9, wherein circuit arrangement is provided in electronic brake systems for motor vehicles or in electronic control systems for governing driving dynamics of motor vehicles, or for controlling electronically controlled parking brakes, or for controlling vehicle restraint systems such as airbag controls (at least see Giers, claim 7).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(**a**) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **9** is rejected under 35 U.S.C. 103(**a**) as being unpatentable over **the cited arts applied to claim 9 above in view of Sayee-Jones et al (Patent/Pub. No.: 5752216)**.

Regarding claim 9, Sayee-Jones discloses an integrated circuit arrangement for safety-critical applications, for controlling tasks in an electronic brake system for motor vehicles, comprising:

a plurality of electronic, cooperating functional groups (25, 25'); and a plurality of electric lines (30) provided to interconnect the functional groups (25, 25'), wherein the functional groups includes groups of a first type and second type, with the functional groups of the first type comprising a functional group redundant microprocessor system (at least see abstract, fig. 1).

Sayee-Jones does not explicitly disclose and the functional group input/output devices (19), and the functional groups of the second type comprising the functional groups actuator drivers (11, 15, 24, 35) and safety circuits (5, 5', 7, 7'), and with the functional groups of the first type and the second type being grouped on a joint chip or chip support member (at least see abstract, fig. 1). However, Adrian et al disclose this limitation, at least see abstract.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Adrian into the disclosure of Sayee-Jones for cost saving.

Claims **9** is rejected under 35 U.S.C. 103(**a**) as being unpatentable over **the cited arts applied to claim 9 above.**

Regarding claim 12, None of the art cited above disclose the integrated circuit arrangement according to claim 9, wherein the electric lines (30) leading from a first functional group (25) to a second functional group (25') are protected by at least one of buffer element(s) (28) or ESD protective structures (29, 29') against fault-producing events of the neighboring functional group(s) and/or against fault-producing outside influences (at least see Giers, abstract).

However, it's well known in the art that an ESD protective structure is require to protect electronic chips and device from been damaged when handled during manufacturing and also to meet the electrical magnetic compatibility.

Regarding claim 13, none of the art cited above disclose the integrated circuit arrangement according to claim 12, wherein the electric lines include the buffer element or the ESD protective structure on at least one or on each side of an isolated area.

However, it's well known in the art that an ESD protective structure is require to protect electronic chips and device from been damaged when handled during manufacturing and also to meet the electrical magnetic compatibility.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELAL A. ALGAHAIM whose telephone number is (571)270-5227. The examiner can normally be reached on Monday - Friday from 7:30 AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HELAL A ALGAHAIM/
Primary Examiner, Art Unit 3663